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10/615,101	07/08/2003	Michael A. Filippo	5500-89400	8643

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MEYERTONS, HOOD, KIVLIN, KOWERT & GOETZEL (AMD)
P.O. BOX 398
AUSTIN, TX 78767-0398

EXAMINER
JOHNSON, BRIAN P

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 06/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

	Application No.	Applicant(s)
Office Action Summary	10/615,101	FILIPPO ET AL.
	Examiner	Art Unit	
	Dillon J. Cody	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>17 April 2006</u>.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-31</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-31</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date <u>27 February 2006</u>.

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

1.   Claims 1-31 are pending.

Papers Filed

2.   Examiner acknowledges receipt of amended claims, and amended specification,

all filed 17 April 2006 and information disclosure statement filed 27 February 2006.

New Rejections

Claim Rejections - 35 USC § 102

3.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public
> use or on sale in this country, more than one year prior to the date of application for patent in the United
> States.

4.   Claims 1-3, 5-6, 8-22, 24-25 and 27-31 are rejected under 35 U.S.C. 102(b) as

being anticipated by Hughes (International Application WO 01/35212) which was cited

on Applicant's information disclosure statement filed 27 February 2006.

5.   As per claims 1 and 14, Hughes discloses a microprocessor and computer

system, comprising: a dispatch unit configured to dispatch load and store operations

(page 12 lines 6-12); and a load store unit configured to store information associated

with load and store operations dispatched by the dispatch unit (Fig. 1), wherein the load

store unit includes a STLF (Store-to-Load Forwarding) buffer (Fig. 1), wherein the STLF

buffer includes a plurality of entries (Fig. 1 and page 15 lines 24-28); wherein the load

store unit is configured to generate an index dependent on at least a portion of an

address of a load operation, to use the index to select one of the plurality of entries, and

to forward data included in the one of the plurality of entries as a result of the load

operation. (page 34 lines 21-30 and claims 1-2)

6.   As per claims 2 and 15, Hughes discloses the microprocessor of claim 1 and

computer system of claim 14, wherein the load store unit is configured to not forward

the data included in the one of the plurality of entries as the result of the load operation

if information included in the one of the plurality of entries does not match information

associated with the load operation. (page 34 lines 21-30 and claims 1-2) *The examiner*

asserts that if the address does not match, an entry is not forwarded on a data load

operation.

7.   As per claims 3 and 22, Hughes discloses the microprocessor of claim 1 and the

method of claim 20, wherein the one of the plurality of entries in the STLF buffer is

configured to store an address, data, and a data size (Fig. 1) associated with a store

operation.

8.   As per claims 5, 16 and 24, Hughes discloses the microprocessor of claim 1,

computer system of claim 14 and the method of claim 20, wherein the load store unit is

configured to select which one of the plurality of entries to allocate to a store operation

by generating an additional index dependent on at least a portion of an address of the store operation. (Fig 1 ADDR - Tag)

9.   As per claims 6, 17 and 25, Hughes discloses the microprocessor of claim 5, computer system of claim 14 and the method of claim 24; wherein the load store unit is configured to generate the additional index dependent on both the at least the portion of the address of the store operation and a number of bytes of data operated on by the store operation, and wherein the load store unit is configured to generate the index dependent on both the at least a portion of the address of the load operation and a number of bytes of data operated on by the load operation. (Page 8 lines 10-13) *The examiner asserts that the data size is used as an index to determine if a TRAP signal is to be generated due to a load requesting a larger block of data than was previously stored at that memory location.*

10.   As per claims 8 and 27, Hughes discloses the microprocessor of claim 5 and the method of claim 24, wherein the additional index comprises a portion of the address targeted by the store operation. (Fig 1 ADDR - Tag)

11.   As per claims 9 and 18, Hughes discloses the microprocessor of claim 1 and computer system of claim 14, wherein the load store unit further comprises a STLF checker configured to verify operation of the STLF buffer. (Fig. 1 Hit control Circuit 402 and page 2 lines 28-32)

12.   As per claims 10 and 28, Hughes discloses the microprocessor of claim 9 and

the method of claim 20, wherein the STLF checker is configured to perform an

associative address comparison to identify all issued store operations targeting a same

address as the load operation and to implement a find-first algorithm to select a

youngest issued store operation that is older than the load operation. (Page 8 lines 14-

17)

13.   As per claims 11, 19 and 29, Hughes discloses the microprocessor of claim 9,

computer system of claim 14 and the method of claim 28, wherein the STLF checker is

configured to replay the load operation if the STLF checker identifies incorrect operation

of the STLF buffer. (Page 5 lines 15-18)

14.   As per claims 12 and 30, Hughes discloses the microprocessor of claim 9 and

the method of claim 28, wherein the STLF checker is configured to replay one or more

additional operations that are dependent on the load operation if the STLF checker

detects incorrect operation of the STLF buffer. (Page 5 lines 15-18) *The examiner*

asserts that after an initial load instruction is attempted and fails, any other instructions

which have been issued which depend on the load instruction for data must be replayed

once the data has been made available through the replay of the load operation.

15.   As per claims 13 and 31, Hughes teaches the microprocessor of claim 9, wherein

the load store unit is configured to identify the result of the load operation as a

speculative value in response to forwarding the data in the one of the plurality of entries

included in the STLF buffer as the result of the load operation; wherein if the STLF

checker verifies that the STLF buffer operated correctly for the load operation, the load

store unit is configured to indicate that the result of the load operation is not speculative.

(abstract and claims 1-4)

16.   As per claim 20, Hughes discloses a method, comprising: receiving an address

of a load operation; generating an index corresponding to the address; using the index

to select an entry from a plurality of entries included in a STLF (Store-to-Load

Forwarding) buffer; and forwarding data included the entry as a result of the load

operation. (abstract, Fig. 1 and page 15 lines 24-28)

17.   As per claim 21, Hughes discloses the method of claim 20, wherein said

forwarding is dependent on information included in the entry matching information

associated with the load operation. *The examiner asserts that the forwarding of an*

entry is dependant on the physical address matching.

Claim Rejections - 35 USC § 103

18.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

19.   Claims 4 and 23, are rejected under 35 U.S.C. 103(a) as being unpatentable

over Hughes.

20.   As per claims 4 and 23, Hughes discloses the microprocessor of claim 1 and the

method of claim 20, but fails to disclose each of the plurality of entries in the STLF

buffer has a capacity to store a maximum amount of data that can be written by a store

operation. Hughes does not disclose the data bus width of the processor of his

invention.

21.   Official Notice is taken that data buses of sizes 8, 16, 32 or 64-bit are extremely

well known in the art. With any of these data buses in place in Hughes' invention, the

data buffer would be able to hold at least the maximum amount of data specified by a

data store operation.

22.   A data bus having a given size less than or equal to 64 bits is beneficial in a

processor in that costs of implementation are limited. Larger data buses require

processor components to also grow in size, increasing processor area, power

consumption and cost.

23.   Implementing a data bus less than or equal to 64 bits in Hughes' invention would

have been obvious at the time of invention to one of ordinary skill in the art for the

benefit of limiting costs, size and power consumption.

24.   Claims 7 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Hughes in view of Hennessy (Hennessy, J. L., Patterson, D. A. Computer Organization

and Design. Morgan Kaufmann Publishers, Inc.: 1998. Pages 549-550.)

25.   As per claims 7 and 26, Hughes discloses the microprocessor of claim 6 and the

method of claim 25, but fails to disclose that the additional index is generated by right-

shifting a lower portion of the address targeted by the store operation by an amount

equal to a logarithm in base two of the number of bytes of data operated on by the store

operation.

26.   Hennessy discloses indexing a cache by means of the lower portion of an

address, minus the appropriate offset for minimum memory access size (byte, in

Hennessy's case) (Fig. 7.7 and page 549-550) Right shifting is an extremely well-

known method of eliminating undesired bits to the right of desired bits.

27.   Hennessy teaches that removing the two bits for the byte offset reduces the total

cache size, as fewer bits must be kept in the tag field of each entry. A smaller cache

size takes up less space on chip and is less expensive to implement.

28.   It would have been obvious to one of ordinary skill in the art at the time of

invention to have included the method of generating a cache index disclosed by

Hennessy in Hughes' invention for the benefit of reducing necessary cache size.

Maintained Rejections

29.   Applicant has failed to overcome the prior art rejections set forth in the previous

Office Action. Consequently, these rejections are respectfully maintained by the

examiner and are copied below for applicant's convenience.

Claim Rejections - 35 USC § 102

30.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

31.   Claims 1-3, 5-6, 8-12, 14-22, 24-25 and 27-30 are rejected under 35

U.S.C. 102(b) as being anticipated by Webb et al. (U.S. Patent No. 6,360,314)

hereinafter referred to as Webb.

32.   As per claims 1 and 14, Webb discloses a microprocessor and computer system,

comprising: a dispatch unit configured to dispatch load and store operations (Fi.g 1

clock cycle: Issue) *The examiner asserts that a unit is responsible for issuing*

operations; and a load store unit configured to store information associated with load

and store operations dispatched by the dispatch unit (Fig. 4), wherein the load store unit

includes a STLF (Store-to-Load Forwarding) buffer (Fig. 4 buffer 428 and queue 426),

wherein the STLF buffer includes a plurality of entries (Fig. 7); wherein the load store

unit is configured to generate an index dependent on at least a portion of an address of

a load operation, to use the index to select one of the plurality of entries (Col. 5 lines 5-8

and 19-22), and to forward data included in the one of the plurality of entries as a result

of the load operation. (Col. 2 lines 8-15)

33.   As per claims 2 and 15, Webb discloses the microprocessor of claim 1 and

computer system of claim 14, wherein the load store unit is configured to not forward

the data included in the one of the plurality of entries as the result of the load operation

if information included in the one of the plurality of entries does not match information

associated with the load operation. (Col. 2 lines 7-15) *The examiner asserts that if the*

address does not match, an entry is not forwarded on a data load operation.

34.   As per claims 3 and 22, Webb discloses the microprocessor of claim 1 and the

method of claim 20, wherein the one of the plurality of entries in the STLF buffer (Fig. 7)

is configured to store an address (Fig. 7 address 42), data (Fig. 7 word 52), and a data

size (Fig. 7 size 48) associated with a store operation.

35.   As per claims 5, 16 and 24, Webb discloses the microprocessor of claim 1,

computer system of claim 14 and the method of claim 20, wherein the load store unit is

configured to select which one of the plurality of entries to allocate to a store operation

by generating an additional index dependent on at least a portion of an address of the

store operation. (Col. 5 lines 5-8 and 19-23)

36.   As per claims 6, 17 and 25, Webb discloses the microprocessor of claim 5,.

computer system of claim 14 and the method of claim 24, wherein the load store unit is

configured to generate the additional index dependent on both the at least the portion of

the address of the store operation (Col. 5 lines 5-8 and 19-23) and a number of bytes of

data operated on by the store operation (Col. 6 lines 51-59), and wherein the load store

unit is configured to generate the index dependent on both the at least a portion of the

address of the load operation and a number of bytes of data operated on by the load

operation. *The examiner asserts that the data size is used as an index to determine if a*

TRAP signal is to be generated due to a load requesting a larger block of data than was

previously stored at that memory location.

37.   As per claims 8 and 27, Webb discloses the microprocessor of claim 5 and the

method of claim 24, wherein the additional index comprises a portion of the address

targeted by the store operation. (Col. 5 lines 19-22)

38.   As per claims 9 and 18, Webb discloses the microprocessor of claim 1 and

computer system of claim 14, wherein the load store unit further comprises a STLF

checker configured to verify operation of the STLF buffer. *The examiner asserts that*

Webb's invention contains a unit which verifies operation, specified as the apparatus

disclosed in col. 7, lines 5-8.

39.   As per claims 10 and 28, Webb discloses the microprocessor of claim 9 and the

method of claim 20, wherein the STLF checker is configured to perform an associative

address comparison to identify all issued store operations targeting a same address as

the load operation and to implement a find-first algorithm to select a youngest issued

store operation that is older than the load operation. (Col. 7 lines 3-36)

40.   As per claims 11, 19 and 29, Webb discloses the microprocessor of claim 9,

computer system of claim 14 and the method of claim 28, wherein the STLF checker is

configured to replay the load operation if the STLF checker identifies incorrect operation

of the STLF buffer. (Col. 1 lines 34-38) *The examiner asserts that if a load operation*

does not result in data being provided from the cache, the memory load is replayed to

main memory.

41.   As per claims 12 and 30, Webb discloses the microprocessor of claim 9 and the

method of claim 28, wherein the STLF checker is configured to replay one or more

additional operations that are dependent on the load operation if the STLF checker

detects incorrect operation of the STLF buffer. (Col. 7 lines 63-65) *The examiner*

asserts that after the inflight instructions are killed, they must inherently be reissued. If

the instructions are not reissued, the program may produce undesired output or simply

cease operation.

42.   As per claim 20, Webb discloses a method, comprising: receiving an address of

a load operation; generating an index corresponding to the address; using the index to

select an entry from a plurality of entries included in a STLF (Store-to-Load Forwarding)

buffer; and forwarding data included the entry as a result of the load operation. (Col. 5

lines 5-22)

43.   As per claim 21, Webb discloses the method of claim 20, wherein said forwarding

is dependent on information included in the entry matching information associated with

the load operation. *The examiner asserts that the forwarding of an entry is dependant*

on the physical address matching.

Claim Rejections - 35 USC § 103

44.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

45.   Claims 4 and 23, are rejected under 35 U.S.C. 103(a) as being unpatentable

over Webb.

46.   As per claims 4 and 23, Webb discloses the microprocessor of claim 1 and the

method of claim 20, but fails to disclose each of the plurality of entries in the STLF

buffer has a capacity to store a maximum amount of data that can be written by a store

operation. Webb further discloses the data entry to hold any of a quadword, longword,

word or byte (Col. 4 line 66-67) but does not disclose the data bus width of the

processor of his invention.

47.   Official Notice is taken that data buses of sizes 8, 16, 32 or 64-bit are extremely

well known in the art. With any of these data buses in place in Webb's invention, the

data buffer would be able to hold at least the maximum amount of data specified by a

data store operation.

48.   A data bus having a given size less than or equal to 64 bits is beneficial in a

processor in that costs of implementation are limited. Larger data buses require

processor components to also grow in size, increasing processor area, power

consumption and cost.

49.   Implementing a data bus less than or equal to 64 bits in Webb's invention would

have been obvious at the time of invention to one of ordinary skill in the art for the

benefit of limiting costs, size and power consumption.

50.   Claims 7 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Webb in view of Hennessy (Hennessy, J. L., Patterson, D. A. Computer Organization

and Design. Morgan Kaufmann Publishers, Inc.: 1998. Pages 549-550.)

51.   As per claims 7 and 26, Webb discloses the microprocessor of claim 6 and the

method of claim 25, but fails to disclose that the additional index is generated by right-

shifting a lower portion of the address targeted by the store operation by an amount

equal to a logarithm in base two of the number of bytes of data operated on by the store

operation.

52.   Hennessy discloses indexing a cache by means of the lower portion of an

address, minus the appropriate offset for minimum memory access size (byte, in

Hennessy's case) (Fig. 7.7 and page 549-550) Right shifting is an extremely well-

known method of eliminating undesired bits to the right of desired bits.

53.   Hennessy teaches that removing the two bits for the byte offset reduces the total

cache size, as fewer bits must be kept in the tag field of each entry. A smaller cache

size takes up less space on chip and is less expensive to implement.

54.   It would have been obvious to one of ordinary skill in the art at the time of

invention to have included the method of generating a cache index disclosed by

Hennessy in Webb's invention for the benefit of reducing necessary cache size.

Response to Arguments

55.   Objections to specification and title are withdrawn in favor of applicant's

amendments and remarks filed 17 April 2006. The examiner notes that the Office may

require a change in title should the scope of the claimed invention change through

future prosecution.

56.   The examiner thanks applicant for pointing out his typo in rejection of claims 5,

16 and 24. Prior rejection has been corrected above.

57.   Applicant's arguments filed on 17 April 2006 have been fully considered but they

are not persuasive.

58.   Applicant argues the novelty/rejection of claims 1, 5, 14 and 20 on pages 9-11 of

the remarks, in substance that:

    "Webb does not disclose a load store unit configured to store information

associate[d] with load and store operations, nor including a Store-to-Load Forwarding

(STLF) buffer."

    "Webb does not disclose the load store unit generating an index and using the

index to select one of the entries in the STLF buffer."

59.   These arguments are not found persuasive for the following reasons:

60.   Webb's invention discloses a buffer to temporarily hold pending store operations

and to forward data upon a subsequent load. For this functionality alone, Webb's

invention contains a "Store-to-Load Forwarding buffer". Further, as disclosed in Fig. 4,

execution unit 418 is dedicated to perform load/store operations and, hence, constitutes

a load/store unit associated with load and store operations. The examiner further notes

that the STLF buffer and associated logic constitute part of the load/store unit as they all

assist in performing load and store operations.

61.   Applicant argues the novelty/rejection of claims 6, 17 and 25 on pages 11-12 of

the remarks, in substance that:

      "The Examiner cites column 6, lines 51-59, as teaching that the index is

generated dependent on the number of bytes of data operated on by the store

operation. While this citation describes a comparison between the size field 48 of a

store queue entry and the size information of an issuing load, it does not describe

generating an index into a STLF buffer dependent on this information."

62.   These arguments are not found persuasive for the following reasons:

63.   As previously cited and applied, the examiner clarifies that the size of the

pending load *is* used as an index to verify the proper data is being loaded from the

buffer. Further, the size of the load is inherently passed into the buffer logic from the

load/store unit and compared, as described in col. 6 lines 51-59. The examiner further

clarifies that both the address portion and the data access size combined constitute the

index described in claim 6. The examiner notes that Webb performs a comparison of

the size as an index in the same manner as the applicant describes in paragraph 36 on

page 12 of the specification.

64.   Applicant argues the novelty/rejection of claims 8 and 27 on page 12 of the

remarks, in substance that:

"Using an address to index into dcache unit 430 teaches nothing about the composition of the additional index (for selecting an entry in the STLF buffer) referred to in Applicants' claim 8."

65.   These arguments are not found persuasive for the following reasons:

66.   The examiner points to Fig. 4 indicating that the additional index generated by the load/store unit is connected to the buffer store queue 426 in addition to dcache 430, as indicated by lines 442 and 446.

67.   Applicant argues the novelty/rejection of claims 9 and 18 on page 13 of the remarks, in substance that:

"column 7, lines 5-8 ... does not describe a unit configured to verify operation of the STLF buffer, as recited in claim 9"

68.   These arguments are not found persuasive for the following reasons:

69.   The examiner clarifies that there must inherently exist logic to verify that the correct entry is forwarded when multiple stores are pending for the same address location. If the youngest store is not forwarded upon a subsequent load, incorrect operation may result.

70.   Applicant argues the novelty/rejection of claims 11, 19 and 29 on pages 13-14 of the remarks, in substance that:

"col. 1 lines 34-38 ... teaches nothing about replaying a load operation."

71.   These arguments are not found persuasive for the following reasons:

72.   The examiner clarifies that when a load misses after a first attempt in the buffer

of Webb's system, the load must be replayed (attempted again) to another memory

device (in this case, the dcache unit 430). There is nothing in applicant's specification

defining the term "replay" and hence, it has been awarded its broadest reasonable

definition.

73.   Applicant argues the novelty/rejection of claims 12 and 30 on pages 14-15 of the

remarks, in substance that:

    "the Examiner's assertion that one or more additional operations that are

dependent on the load operation must be replayed is mere speculation, not a necessary

condition of operation."

74.   These arguments are not found persuasive for the following reasons:

75.   As previously described, inflight instructions which are killed must inherently be

re-issued if proper program outcome is to be achieved. As described by Webb, when

the TRAP signal is issued in the instance described in col. 7, it signals that the load

operation did not provide data when it should have (col. 7 line 34), resulting in incorrect

and/or unavailable data. A program contains instructions in a certain order designed to

achieve a pre-defined function. If a system were to kill the inflight instructions following

a data miss (like that described in col. 7) without reissuing them, the function of the

program may not be achieved.

Conclusion

76.   Applicant's submission of an information disclosure statement under 37 CFR

1.97(c) with the fee set forth in 37 CFR 1.17(p) on 17 April 2006 prompted the new

ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS**

MADE FINAL. See MPEP § 609.04(b)II. Applicant is reminded of the extension of time

policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later

than SIX MONTHS from the mailing date of this final action.

77.   The following is text cited from 37 CFR 1.111(c): In amending in reply to a

rejection of claims in an application or patent under reexamination, the applicant or

patent owner must clearly point out the patentable novelty which he or she thinks the

claims present in view of the state of the art disclosed by the references cited or the

objections made. The applicant or patent owner must also show how the amendments

avoid such references or objections.

    Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dillon Cody whose telephone number is 571-272-8401. The examiner can normally be reached on Mon - Fri, 8 AM - 5 PM EST.

    If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

    Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DJC

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100